NARASIMHA REDDY ENGINEERING COLLEGE
(Autonomous)
Approved by AICTE, New Delhi & Affiliated to JNTUH, Hyderabad
Accredited by NAAC with A Grade, Accredited by NBA

ELECTRONICS AND COMMUNICATION ENGINEERING

QUESTION BANK

Course Title : Digital Logic Design

Course Code : EC2103PC

Regulation : NR21

Course Objectives

1. To understand basic number systems, codes and logical gates.
2. To understand the concepts of Boolean algebra and the use of minimization logic to solve the Boolean logic expressions..
3. To understand the design of combinational and sequential circuits.
4. To understand the state reduction methods for Sequential circuits.
5. To understand the basics of various types of memories.

Course Outcomes (CO's)

CO1: Demonstrate the relation between various number systems and model basic functions based on Boolean algebra and logic gates

CO2: Analyze logic function using K-maps ad tabular method and develop basic combinational digital systems.

CO3: Characterize sequential circuits and design clock based registers and counters.

CO4: Design synchronous and asynchronous finite state machines.

CO5: Compare various digital logic families based on power, speed and interfacing characteristics

UNIT–I

UNIT NAME

S. No	Questions	BT	CO	PO
	Part – A (Short Answer Questions)			
1	Discuss 1's and 2's complement methods of subtraction?	L2	1	1, 2
2	Explain how do you convert AOI logic to NAND logic?	L6	1	1, 2, 3, 4, 5, 6, 12
3	Design self complementary 631-1 codes	L6	1	1, 2, 3, 4, 5, 6, 12
4	Implement AND, OR and NOT gate using NAND Gate	L6	1	1, 2, 3, 4, 5, 6, 12
5	Implement AND, OR and NOT gate using NOR	L6	1	1, 2, 3, 4, 5, 6, 12

		Gate			
6		Convert (3.1415)10 to ()2	L2	1	1, 2
7		Perform the following conversions a. (101101.10101)2 = ()10 b. (0.65625)10 = ()2	L2	1	1, 2
8		Perform the following operations using 2's complement method using 8-bit representation of numbers: a. 48-(-23) b. - 48-23	L2	1	1, 2
9		Prove the following a. xy + xy' = x b. (x+y)(x+y')=x c. x + x'y = x+y d. xy + x'z + yz = xy + x'z e. (x+y)(x'+z)(y+z) = (x+y)(x'+z)	L2	1	1, 2
10		Prove the following: a. $\overline{A \oplus B} = AB + \bar{A}\bar{B}$ b. $A \oplus B = \bar{A} \oplus \bar{B}$ c. $\overline{A \oplus B} = A \oplus \bar{B}$ d. $\overline{A \oplus B} = \bar{A} \oplus B$ e. $B \oplus (B \oplus A.C) = AC$	L3	1	1, 2, 3
Part – B (Long Answer Questions)					
11	a)	A safe has five locks, *v, w, x, y,* and *z,* all of which must be unlocked for the safe to open. The keys to the locks are distributed among five executives in the following manner: *A* has keys for locks *v* and *x*; *B* has keys for locks *v* and *y*; *C* has keys for locks *w* and *y*; *D* has keys for locks *x* and *z*; *E* has keys for locks *v* and *z*. a. Determine the minimum number of executives required to open the safe. b. Find all the combinations of executives that can open the safe. Write an expression *f* (*A,B,C,D,E*) which specifies when the safe can be opened as a function of which executives are present. c. Who is the "essential executive" without whom the safe cannot be opened?	L5	1	1, 2, 3, 4, 5
	b)	Construct Hamming code for BCD 0110. Use even parity.	L6	1	1, 2, 3, 4, 5, 6, 12
12	a)	You are presented with a set of requirements under which an insurance policy will be issued. The applicant must be 1. a married female 25 years old or over, or 2. a female under 25, or 3. a married male under 25 who has not been involved in a car accident, or 4. a married male who has been involved in a car accident, or 5. a married male 25 years or over who has not been involved in a car accident.	L3	1	1, 2, 3

		Variables *w*, *x*, *y*, and *z* assume truth value 1 in the following cases: *w* = 1 if the applicant has been involved in a car accident; *x* = 1 if the applicant is married; *y* = 1 if the applicant is a male; *z* = 1 if the applicant is under 25. a. Find an algebraic expression that assumes the value 1 whenever the policy should be issued. b. Simplify algebraically the above expression and suggest a simpler set of requirements.			
	b)	Simplify (a) (A + C) (A + D) (B + C) (B + D) (b) $A\left(\bar{A} + C\right)\left(\bar{A}B + \bar{C}\right)$ (c) AB + A(B + C) + B (B + C) (d) $ABC + \bar{A}\bar{B}\bar{C} + AB\bar{C} + \bar{A}BC$ (e) $\bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + BC + \bar{A}\bar{B}C + A\bar{B}C$ (f) $\bar{A}BC + \bar{B}CD + AC + \bar{A}\bar{B}C\bar{D}$	L3	1	1, 2, 3
13	a)	Simplify to a sum of 3 terms: A'C'D'+AC'+BCD+A'CD'+A'+AB'C' Given AB' + AB = C, Show that AC' + A'C = B	L3	1	1, 2, 3
	b)	Decimal system became popular because we have 10 fingers. A rich person on earth has decided to distribute Rs. one lakh equally to the following persons from various planets. Find out the amount each one of them will get in their respective currencies: A from planet VENUS possessing 8 fingers B from planet MARS possessing 6 fingers C from planet JUPITER possessing 14 fingers D from planet MOON possessing 16 fingers	L6	1	1, 2, 3, 4, 5, 6, 12
14	a)	Perform the decimal subtraction in 8-4-2-1 BCD using 9's complement Subtract i) 79 from 26 ii) Subtract 748 from 983	L2	1	1, 2
	b)	Simplify the following expression using Boolean algebra rules $\overline{\overline{A\bar{B} + ABC} + A(B + A\bar{B})}$	L3	1	1, 2, 3
15	a)	Check whether the received code 10101100 is correctly received or not if even parity is used.	L6	1	1, 2, 3, 4, 5, 6, 12
	b)	Realize the following function as multilevel NAND-NAND network$f = B(A + CD) + A\bar{C}$	L6	1	1, 2, 3, 4, 5, 6, 12
16	a)	Design 4 bit weighted complementary codes where the weight of the LBS is negative	L6	1	1, 2, 3, 4, 5, 6, 12
	b)	Simplify the following Boolean expressions to a minimum number of literals (i) ABC+A'B+ABC' (ii) xy + x(wz+wz')	L3	1	1, 2, 3

UNIT–II

UNIT NAME

S.No		Questions	BT	CO	PO
Part – A (Short Answer Questions)					
1		Simplify using K-map (a) $\bar{A}B\bar{C} + AB\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}BC + ABC$	L5	2	1, 2, 3, 4, 5
2		Simplify the Boolean function using Kmap $F(W,X,Y,Z) = \sum m(1,3,7,11,15) + d(0,2,5)$	L5	2	1, 2, 3, 4, 5
3		Design 4 bit even parity generator	L6	2	1, 2, 3, 4, 5, 6, 12
4		Design half adder using NAND gate only	L6	2	1, 2, 3, 4, 5, 6, 12
5		Design 4:1 MUX using 2:1 MUX	L6	2	1, 2, 3, 4, 5, 6, 12
6		Design 4 bit Binary to Gray code Converter	L6	2	1, 2, 3, 4, 5, 6, 12
7		Design Half subtractor using NOR gates only	L6	2	1, 2, 3, 4, 5, 6, 12
8		Design comparator to check if two nibbles are equal.	L6	2	1, 2, 3, 4, 5, 6, 12
9		Design 4:1 Demultiplexer using NOR gate only	L6	2	1, 2, 3, 4, 5, 6, 12
10		Design 4-to-2 Bit Binary Encoder	L6	2	1, 2, 3, 4, 5, 6, 12
Part – B (Long Answer Questions)					
11	a)	Implement 4 bit adder/ subtractor circuit	L2	2	1, 2
	b)	Minimize the logic Function Y=Π*M*(0,1,4,6) and realize using NOR gate. Determine whether hazard occurs in this circuit. If yes, find the condition under which it occurs and give the timing diagram. Assume propagation delay of NOR gate 1 to be lower than that of 2.	L5	2	1, 2, 3, 4, 5
12	a)	Design Decimal to BCD encoder	L6	2	1, 2, 3, 4, 5, 6, 12
	b)	Simplify using Quine-McClusky tabulation method f (A, B, C, D) =Σm(1, 3, 7, 11, 15) + d(0, 2, 5)	L3	2	1, 2, 3
13	a)	Simplify using K-map (a) $\bar{A}B\bar{C} + AB\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}BC + ABC$ (b) $B\overline{CD} + \bar{A}B\bar{C}D + AB\bar{C}D + \bar{A}BCD + ABCD$ (c) $\bar{A}\bar{B}\bar{C} + A\overline{CD} + A\bar{B} + ABC\bar{D} + \bar{A}\bar{B}C$ (d) $\bar{B}(CD + \bar{C}) + C\bar{D}(\overline{A + B} + AB)$ (e) $\bar{A}\bar{D} + A\bar{B}\bar{D} + \bar{A}\bar{C}D + \bar{A}CD$	L3	2	1, 2, 3
	b)	Design 8:1 Mux using 4:1 mux using two different implementation schemes.	L6	2	1, 2, 3, 4, 5, 6, 12
14	a)	Design a combinatorial circuit that accepts a three bit number and generates an output Binary number equal to the square of the input number?	L6	2	1, 2, 3, 4, 5, 6, 12
	b)	Construct a 4 to 16 line decoder using 2 to 4 line decoders?	L6	2	1, 2, 3, 4, 5, 6, 12
15	a)	Use a multiplexer having three data select inputs to solve the logic for the function F = Σ (0, 1, 2, 3, 4, 10, 11, 14, 15)	L5	2	1, 2, 3, 4, 5
	b)	Implement the function f(a,b,c)=Σ(1,3,4,6) using NOR-NOR two level gate structure.	L6	2	1, 2, 3, 4, 5, 6, 12

16	a)	Realize a full subtractor using decoders	L6	2	1, 2, 3, 4, 5, 6, 12
	b)	Obtain the simplified expression in SOP form of $F(a,b,c,d,e)=\Sigma(1,2,4,7,12,14,15,24,27,29,30,31)$ using K-maps.	L3	2	1, 2, 3

UNIT–III

UNIT NAME

S.No		Questions	BT	CO	PO
Part – A (Short Answer Questions)					
1		Show the excitation table and truth table of JK flip flop.	L3	3	1, 2, 3
2		Differentiate critical and non-critical race	L4	2	1, 2, 3, 4
3		Discuss the difference between synchronous and asynchronous sequential circuits.	L2	2	1, 2
4		Draw the logic diagram of a master slave J-K flip-flop.	L4	2	1, 2, 3, 4
5		Design SR Flipflop using NOR Gate	L6	2	1, 2, 3, 4, 5, 6, 12
6		Design D flipflop using JK flipflop	L6	2	1, 2, 3, 4, 5, 6, 12
7		Design 4 bit Serial-In-Serial-Out Shift Register	L6	2	1, 2, 3, 4, 5, 6, 12
8		Design mod-8 asynchronous counter using T flipflop	L6	2	1, 2, 3, 4, 5, 6, 12
9		Design Clock divide by 8 circuit	L6	2	1, 2, 3, 4, 5, 6, 12
10		If you have a 50 MHz clock, 1 ns setup time, and 2 ns hold time, what will your design allow for its maximum propagation delay between two flip-flops?	L6	2	1, 2, 3, 4, 5, 6, 12
Part – B (Long Answer Questions)					
11	a)	Design Bounce elimination switch	L6	2	1, 2, 3, 4, 5, 6, 12
	b)	Design 4 bit Ripple counter	L6	2	1, 2, 3, 4, 5, 6, 12
12	a)	Design Mod-6 synchronous counter	L6	2	1, 2, 3, 4, 5, 6, 12
	b)	Design 4 bit Serial-In-Parallel-Out shift register	L6	2	1, 2, 3, 4, 5, 6, 12
13	a)	Design BCD counter	L6	2	1, 2, 3, 4, 5, 6, 12
	b)	Design a MOD-5 synchronous counter using flip flops and implement it? Also draw the timing diagram?	L6	2	1, 2, 3, 4, 5, 6, 12
14	a)	Explain the output frequency of T filp-flop if the input clock frequency is 10khz? Give its timing waveform?	L6	2	1, 2, 3, 4, 5, 6, 12
	b)	Design a ring and twisted ring counter compare their waveforms	L6	2	1, 2, 3, 4, 5, 6, 12
15	a)	Design 4 bit Parallel to serial converter	L6	2	1, 2, 3, 4, 5, 6, 12
	b)	Design a circuit to 1 HZ clock from 1KHz clock signal	L6	2	1, 2, 3, 4, 5, 6, 12
16	a)	Design 4 bit Up Down counter	L6	2	1, 2, 3, 4, 5, 6, 12
	b)	What is the drawback of JK flip flop, design a flip flop which overcomes this drawback and explain with neat diagram.	L6	2	1, 2, 3, 4, 5, 6, 12

UNIT–IV

UNIT NAME

S. No		Questions	BT	CO	PO
Part – A (Short Answer Questions)					
1		Design an FSM based Serial adder	L6	4	1, 2, 3, 4, 5, 6, 12
2		Explain briefly with the difference between the Mealy model and Moore model.	L6	4	1, 2, 3, 4, 5, 6, 12
3		Design an FSM to detect even number of or odd number of 0's or 1's in the given serial input. Use the Moore machine for the design.	L6	4	1, 2, 3, 4, 5, 6, 12
4		Explain the following a) State diagram b) State table c) State Assignment rules d) State Reduction Table	L6	4	1, 2, 3, 4, 5, 6, 12
5		Draw block diagrams of Moore and Mealy model? Explain.	L6	4	1, 2, 3, 4, 5, 6, 12
6		Explain capabilities and limitations of finite state machine.	L6	4	1, 2, 3, 4, 5, 6, 12
7		Compare Moore and Mealy machine and explain the rules for converting Mealy machine to Moore and vice versa?	L6	4	1, 2, 3, 4, 5, 6, 12
8		Design an FSM to detect three or more sequence of 1's.	L6	4	1, 2, 3, 4, 5, 6, 12
9		Design an FSM to calculate 2's complement	L6	4	1, 2, 3, 4, 5, 6, 12
10		Design an FSM of 2 bit UP/DOWN counter	L6	4	1, 2, 3, 4, 5, 6, 12
Part – B (Long Answer Questions)					
11	a)	Draw the state transition diagram and the state transition table of a J-K flip-flop. Explain.	L6	4	1, 2, 3, 4, 5, 6, 12
	b)	Design a Serial Adder using a state transition table and suitable State diagram.	L6	4	1, 2, 3, 4, 5, 6, 12
12	a)	Design a one-input one-output sequence detector that produces an output value 1 every time the sequence 0101 is detected and an output value 0 at all other times.	L6	4	1, 2, 3, 4, 5, 6, 12
	b)	Draw State diagram and state transition table for a modulo-10 binary counter	L4	4	1, 2, 3, 4
13	a)	Design a parity bit generator circuit such that parity bit 1 is to be inserted if and only if the number of 1's in the preceding string of three symbols is odd.	L6	4	1, 2, 3, 4, 5, 6, 12
	b)	Design modulo-6 counter using T Flipflop and draw its state transition table.	L6	4	1, 2, 3, 4, 5, 6, 12
14	a)	Draw the state diagram and state transition table of Self starting decade counter.	L4	4	1, 2, 3, 4
	b)	Design a circuit that detects three consecutive '1's using Mealy and Moore FSM.	L6	4	1, 2, 3, 4, 5, 6, 12
15	a)	Design an FSM- finite state machine to check whether the two inputs A and B have the same value for the previous three samples. Use Mealy machine for the design.	L6	4	1, 2, 3, 4, 5, 6, 12
	b)	Design a sate reduced FSM using the FSM given below	L6	4	1, 2, 3, 4, 5, 6, 12

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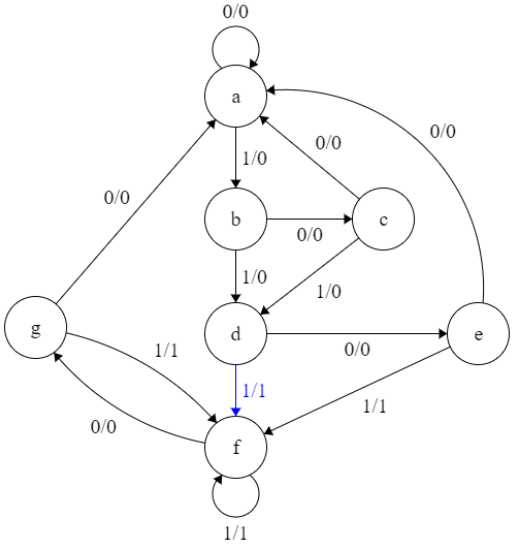
<td> 
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<td>16</td>
<td>a)</td>
<td>Given the conditions, such that
If A = 0, the circuit oscillates between either one of the two cases. Case 1: 00-01-00-01… and Case 2: 10-11-10-11… And
If A = 1, it switches inter between two cases. Draw the state transition diagram and implement the same using JK flip-flop and by using basic logic gates</td>
<td>L4</td>
<td>4</td>
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<td>b)</td>
<td>Optimize or simplify the following given truth table. Given the input sequence 01010101001. Start from the state a and write the next state and output sequence for both original and optimized tables.
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<tr><td rowspan="2">PS</td><td colspan="2">NS</td><td colspan="2">Output</td></tr>
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<tr><td>a</td><td>a</td><td>b</td><td>0</td><td>0</td></tr>
<tr><td>b</td><td>e</td><td>c</td><td>0</td><td>1</td></tr>
<tr><td>c</td><td>a</td><td>d</td><td>0</td><td>1</td></tr>
<tr><td>d</td><td>e</td><td>f</td><td>0</td><td>1</td></tr>
<tr><td>e</td><td>a</td><td>f</td><td>0</td><td>0</td></tr>
<tr><td>f</td><td>g</td><td>d</td><td>0</td><td>1</td></tr>
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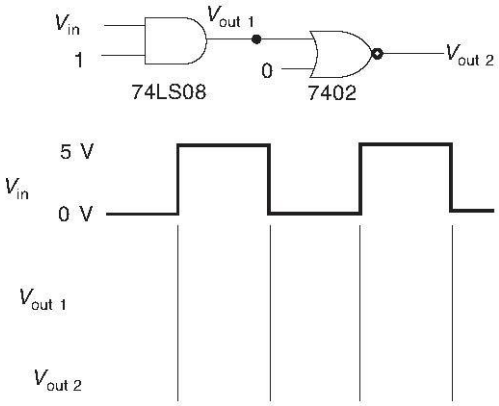
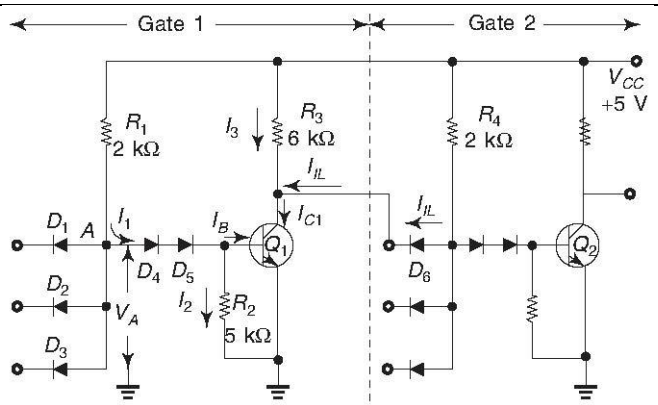
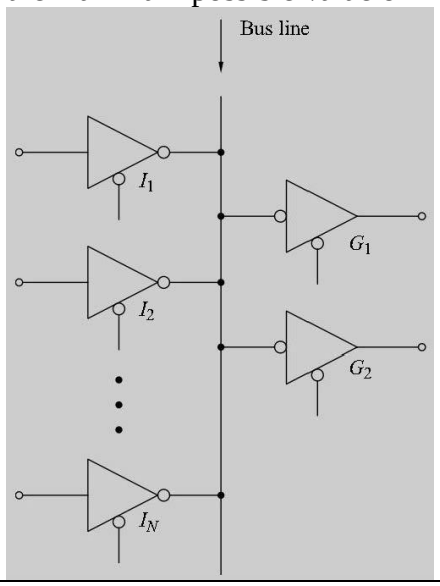
UNIT–V

UNIT NAME

S. No		Questions	BT	CO	PO
Part – A (Short Answer Questions)					
1		Define Propagation delay and Power dissipation in Logic Families	L1	5	1
2		Define Fan-in & Fan-out.	L1	5	1
3		What is Noise margin and Figure of Merit?	L3	5	1, 2, 3
4		State the advantages and disadvantages of TTL logic family.	L1	5	1
5		What is the effect of increasing the supply voltage on the propagation delay of the CMOS gates	L1	5	1
6		Which IC family offers a) lowest propagation delay and b) lowest power dissipation.	L1	5	1
7		List the characteristics of the digital ICs	L1	5	1
8		Compare the current spikes in ECL and TTL gates	L5	5	1, 2, 3, 4, 5
9		The propagation delay times for a 74LS08 AND gate (Fig. below) are tPLH = 15 ns, tPHL = 20 ns and for a 7402 NOR gate they are LPLH = 22 ns, tPHL = 15 ns. Sketch Vout1 and Vout2 showing the effects of propagation delay. Assume 0 ns for rise and fall times. 	L3	5	1, 2, 3
10		Illustrate TTL and CMOS logic levels	L5	5	1, 2, 3, 4, 5
Part – B (Long Answer Questions)					
11	a)	Illustrate the effects of input noise on gate operation.	L5	5	1, 2, 3, 4, 5
	b)	Draw the circuit of 2 input CMOS NAND gate and explain it's operation with waveform	L6	5	1, 2, 3, 4, 5, 6, 12
12	a)	Draw the circuit of 2 input CMOS NOR gate and explain it's operation with waveform	L6	5	1, 2, 3, 4, 5, 6, 12
	b)	Determine the fan-out for the DTL NAND gate shown in Fig. Assume that transistors Q1 and Q2 have hFE(min) = 20 and that all diodes and transistors are silicon.	L5	5	1, 2, 3, 4, 5

					
13	a)	Describe the basic circuitry of a three-input TTL gate.	L2	5	1, 2
	b)	Describe tristate logic (TSL). Draw and explain the circuit of a TSL NAND gate	L6	5	1, 2, 3, 4, 5, 6, 12
14	a)	Explain in detail the significance of noise margins of a gate.	L6	5	1, 2, 3, 4, 5, 6, 12
	b)	Describe how the problem of a variable load is overcome by the totem-pole arrangement	L6	5	1, 2, 3, 4, 5, 6, 12
15	a)	A wired-AND circuit is to drive the inputs of five TTL gates. Determine a suitable pull-up resistor. (IIL(max) = 1.6mA and IOL(max) = 16mA)	L5	5	1, 2, 3, 4, 5
	b)	Briefly explain high-threshold logic. Give its specifications	L6	5	1, 2, 3, 4, 5, 6, 12
16	a)	Consider the arrangement shown below. At any time one of the gates drives the bus line. Calculate the maximum possible value of *N*. 	L6	5	1, 2, 3, 4, 5, 6, 12
	b)	Draw the logic diagram of a master-slave D flipflop using transmission gates and inverters.	L4	5	1, 2, 3, 4

* **Blooms Taxonomy Level (BT)** (L1 – Remembering; L2 – Understanding; L3 – Applying; L4 – Analyzing; L5 – Evaluating; L6 – Creating)

Course Outcomes (CO)

Program Outcomes (PO)

Prepared By: **HOD, ECE**