I. Syllabus

EC2103PC: DIGITAL LOGIC DESIGN

B. Tech. II Year I Sem.	L	T	P	C
Pre-Requisites: Nil	3	1	0	4

Course Objectives:

1. To understand common forms of number representation in logic circuits
2. To learn basic techniques for the design of digital circuits and fundamental concepts used in the design of digital systems.
3. To understand the concepts of combinational logic circuits and sequential circuits.
4. To understand the Realization of Logic Gates Using Diodes & Transistors.

Course Outcomes: Upon completing this course, the student will be able to

1. Demonstrate the relation between various number systems and model basic functions based on Boolean algebra and logic gates
2. Analyze logic function using K-maps ad tabular method and develop basic combinational digital systems.
3. Characterize sequential circuits and design clock based registers and counters.
4. Design synchronous and asynchronous finite state machines.
5. Compare various digital logic families based on power, speed and interfacing characteristics

UNIT - I:

Number Systems: Number systems, Complements of Numbers, Codes- Weighted and Non-weighted codes and its Properties, Parity check code and Hamming code.

Boolean Algebra: Basic Theorems and Properties, Switching Functions- Canonical and Standard Form, Algebraic Simplification, Digital Logic Gates, EX-OR gates, Universal Gates, Multilevel NAND/NOR realizations.

UNIT - II:

Minimization of Boolean functions: Karnaugh Map Method - Up to five Variables, Don't Care Map Entries, Tabular Method,

Combinational Logic Circuits: Adders, Subtractors, Comparators, Multiplexers, Demultiplexers, Encoders, Decoders and Code converters, Hazards and Hazard Free Relations.

UNIT - III

Sequential Circuits Fundamentals: Basic Architectural Distinctions between Combinational and Sequential circuits, SR Latch, Flip Flops: SR, JK, JK Master Slave, D and T Type Flip Flops, Excitation Table of all Flip Flops, Timing and Triggering Consideration, Conversion from one type of Flip-Flop to another.

Registers and Counters: Shift Registers – Left, Right and Bidirectional Shift Registers, Applications of Shift Registers - Design and Operation of Ring and Twisted Ring Counter, Operation of Asynchronous and Synchronous Counters.

UNIT - IV

Sequential Machines: Finite State Machines, Synthesis of Synchronous Sequential Circuits- Serial Binary Adder, Sequence Detector, Parity-bit Generator, Synchronous Modulo N –Counters. Finite state machine-capabilities and limitations, Mealy and Moore models.

UNIT - V

Realization of Logic Gates Using Diodes & Transistors: AND, OR and NOT Gates using Diodes and Transistors, DCTL, RTL, DTL, TTL, CML and CMOS Logic Families and its Comparison,

Classification of Integrated circuits, comparison of various logic families, standard TTL NAND Gate- Analysis & characteristics, TTL open collector O/Ps, Tristate TTL, MOS & CMOS open drain and tri- state outputs, CMOS transmission gate, IC interfacing- TTL driving CMOS & CMOS driving TTL.

TEXT BOOKS:

1. Switching and Finite Automata Theory - Zvi Kohavi & Niraj K. Jha, 3rd Edition, Cambridge, 2010.
2. Modern Digital Electronics – R. P. Jain, 3rd Edition, 2007- Tata McGraw-Hill

REFERENCE BOOKS:

1. Digital Design- Morris Mano, PHI, 4th Edition,2006
2. Introduction to Switching Theory and Logic Design – Fredriac J. Hill, Gerald R. Peterson, 3rd Ed, John Wiley & Sons Inc.
3. Fundamentals of Logic Design- Charles H. Roth, Cengage Learning, 5th, Edition, 2004.
4. Switching Theory and Logic Design – A Anand Kumar, PHI, 2013

II. CO/PO mapping

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	3	1	2	1	-	-	-	-	-	2
CO2	3	2	2	1	2	1	-	-	-	-	-	2
CO3	2	3	3	2	2	1	-	-	-	-	-	2
CO4	3	2	1	1	1	-	-	-	-	-	-	2
CO5	3	3	3	2	2	1	-	-	-	-	-	3
Average	2.8	2.4	2.4	1.4	1.8	1						2.2

MAPPING OF COURSE OUTCOMES WITH PSO's

Course	PSO1	PSO2	PSO3
CO1	3	2	3
CO2	3	2	2
CO3	3	3	3
CO4	3	2	1
CO5	3	3	3
Average	3	2.4	2.4